

AMENDMENTS TO THE SPECIFICATION

Please replace the abstract with the following:

~~Signal dynamic range in a CMOS active pixel is increased by using separate set and reset lines. An image sensing device, such as a CMOS Active Pixel Sensor device, including an array of pixels. Each pixel has a photoreceptor, a follower transistor connected to the photoreceptor, a select transistor connected to the follower transistor, and a reset transistor. A first bias line provides power to at least a first of the transistors for a first pixel, and a second bias line provides power to at least a second of the transistors of said first pixel different than the first transistor of the first pixel.~~

Please replace the second full paragraph on page 6 with the following:

After signal sampling is completed, the voltage on VDD line N-1 drops to 0 at 224 during the reset time for photodiode [[223]] 220 for line N-1. This means that the floating diffusion for that photodiode [[223]] 220 will be charged to the reset level when the output column is grounded and the surface potential under the source follower gate is minimum. This may increase the cell capacitance.

Please replace the first full paragraph on page 7 with the following:

The line 230 shows the photodiode boosting that occurs. During the reset pulse, the output is boosted by an amount 232. Importantly, the drains of the reset transistor [[216]] 225 and the source follower 215 for the same photodiode are connected to different VDD lines. The joint VDD contact for the reset transistor drain of one photodiode is connected to the source follower drain of another photodiode. For example, Figure 2 shows the gate of source follower 215 being connected to the drain of

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the reset transistor 225 for a separate line. This layout can save pixel space, provide improve improved FF, quantum efficiency, and have a relatively small pixel pitch.